

EXHIBIT 2

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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13/288,850

11/03/2011

Hyun Lee

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EXAMINER

HOANG, HUAN

ART UNIT

PAPER NUMBER

2827

NOTIFICATION DATE

DELIVERY MODE

10/11/2013

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jz@jzpatent.com

Office Action SummaryApplication No.
13/288,850Applicant(s)
LEE, HYUNExaminer
HUAN HOANGArt Unit
2827AIA (First Inventor to File)
Status
No**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --****Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____.; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 5) ☒ Claim(s) 1-34 is/are pending in the application.
 5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 1-7,9-21 and 23-34 is/are rejected.
- 8) ☒ Claim(s) 8 and 22 is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 11/03/11 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some * c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08)
 Paper No(s)/Mail Date 05/23/12, 04/25/13
- 3) ☐ Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
- 4) ☐ Other: _____.

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plurality of array dies; and the second data conduit has a second load is less than a load that would be on the second data conduit upon the second die interconnect being placed in electrical communication with at least one data port of each of the array dies of the plurality of array dies.“ is confusing since the first die interconnect/the second die interconnect is only in electrical communication with the first group of array dies/the second group of at least one die; therefore, the first die interconnect/the second die interconnect cannot be in electrical communication with each of the array dies (at least one array die of the second group is not in electrical communication with the first die interconnect and the array dies of the first group are not in electrical communication with the with the second die interconnect).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4, 7, 9-13, 15-21, 23, 24, 27-29, 31, 33 and 34 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Rajan et al. (US 2008/0025137).

Regarding claim 1: Rajan (Fig. 2B) shows a memory package, comprising:

a plurality of input/output terminals (address, Control, Clock and Data) via which the memory package communicate data and control/address signals with one or more external devices;

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a plurality of stacked array dies (paragraph [0043], lines 1-3) including a first group of array dies (206A and 206C) and a second group (206B and 206D) of at least one array die, each array die having data ports;

at least a first die interconnect (Data connected to 206A and 206C) and a second die interconnect (Data connected to 206B and 206D), the first die interconnect in electrical communication with first group of array dies and not in electrical communication with the second group of at least one array die, the second die interconnect in electrical communication with the second group of at least one array die and not in electrical communication with the first group of array dies; and

a control die (BUFFER CHIP) comprising at least a first data conduit between the first die interconnect and a first terminal (Data) of the plurality of input/output terminals, and at least a second data conduit between the second die interconnect and the first terminal, the first terminal being a data terminal, the control die further comprising a control circuit (paragraph [0044], lines 5-7) to control respective states of the first data conduit and the second data conduit in response to control signals received via one or more second terminals of the plurality of terminals (Address, Clock and Control).

Regarding claims 2-4: Rajan discloses the memory package of claim 1, wherein the control signals include data path control signals (Control, Address and Clock must be used to address the DRAM circuits and control the data between Data terminal to DRAM circuits) for controlling the first and second data conduits.